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VERIFICATION

I, Keisaku NAKAO,
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This 15 day of April, 2004

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[Document Name] PATENT APPLICATION

[Identification No.] 74112154

[Filing date] February 19, 2001

[To] Commissioner of Japanese Patent Office

[International Patent Classification] H01L 27/00

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[Indication of Charge]

[Deposit Payment Register Number] 053213

[Amount of Fee] 21000yen

[Items of the Filing Articles]

[Article Name] Specification one copy

[Article Name] Drawings one copy

[Article Name] Abstract one copy

[General Power of Attorney] 9715177

[Proof] Necessary

[Document Name] Specification

[Title of the invention] SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOOD OF THE SAME

[Scope of Patent to be Claimed]

[Claim 1]

A semiconductor memory device comprising:

a MOS transistor formed in a surface portion of a semiconductor substrate, wherein said MOS transistor has a gate, a source region, and a drain region;

a first insulating film covering said MOS transistor;

a capacitor section formed on said first insulating film, wherein said capacitor section includes a bottom electrode, a dielectric layer formed on said bottom electrode, an upper electrode formed on said dielectric layer; and

a first contact portion formed through said first insulating film to extend from said bottom electrode to said source region, wherein said first contact portion includes a first metal plug portion.

[Claim 2]

The semiconductor memory device according to Claim 1, wherein said first metal plug portion includes a barrier metal layer formed in side and bottom portions thereof, and a refractory metal layer formed inside said barrier metal layer.

[Claim 3]

The semiconductor memory device according to Claim 1

or Claim 2, wherein said barrier metal layer is a first titanium nitride layer and said refractory metal layer is a first tungsten layer.

[Claim 4]

The semiconductor memory device according to any of Claims 1 to 3, wherein said capacitor section is formed to extend from a surface to inside of said first insulating film, and to thereby have a trench structure.

[Claim 5]

The semiconductor memory device according to any of Claims 1 to 4, wherein said capacitor section is formed perpendicularly above said source region.

[Claim 6]

The semiconductor memory device according to any of Claims 1 to 5, wherein said bottom electrode has a laminate structure of a titanium nitride layer and a doped polysilicon layer.

[Claim 7]

The semiconductor memory device according to any of Claims 1 to 6, wherein said upper electrode has a laminate structure of the titanium nitride layer and the doped polysilicon layer.

[Claim 8]

The semiconductor memory device according to any of Claims 1 to 7, wherein said dielectric layer is formed with high dielectric constant material.

[Claim 9]

The semiconductor memory device according to any of

Claims 1 to 8, further comprising a second contact portion formed in the upper perpendicular direction from said drain region through said first insulating film to include a second metal plug portion.

[Claim 10]

The semiconductor memory device according to Claim 9, wherein said second metal plug portion includes a second titanium nitride layer formed in side and bottom portions, and a second tungsten layer formed inside said second titanium nitride layer.

[Claim 11]

The semiconductor memory device according to any of Claims 1 to 10, further comprising:

a second insulating film which covers said capacitor section and said first insulating film, and

a third contact portion which extends from a surface of said second insulating film to said second contact portion at said first insulating film.

[Claim 12]

The semiconductor memory device according to Claim 11, wherein said second contact portion and said third contact portion function as a bit line.

[Claim 13]

A semiconductor memory device comprising:

a first MOS transistor formed in a first surface portion of a semiconductor substrate, wherein said first MOS transistor has a first gate, a first source region, and a drain region;

a second MOS transistor formed in a second surface portion of said semiconductor substrate, wherein said second MOS transistor has a second gate, a second source region, and said drain region, in which said drain region is shared by said first MOS transistor and said second MOS transistor;

a first insulating film covering said first MOS transistor and said second MOS transistor;

a first capacitor section formed on said first insulating film to have a trench structure, wherein said first capacitor includes a first bottom electrode, a first dielectric layer formed on said first bottom electrode, and a first upper electrode formed on said first dielectric layer;

a second capacitor formed on said first insulating film to have a trench structure, wherein said second capacitor includes a second bottom electrode, a second dielectric layer formed on said second bottom electrode, and a second upper electrode formed on said second dielectric layer;

a first contact portion formed on said first insulating film to extend from said first bottom electrode to said first source region; and

a second contact portion formed on said first insulating film to extend from said second bottom electrode to said second source region, wherein each of said first contact portion and said second contact portion includes a first metal plug portion.

[Claim 14]

The semiconductor memory device according to Claim 13, wherein said first metal plug portion includes a barrier metal layer formed within side and bottom portions thereof and a refractory metal layer formed inside said barrier metal layer.

[Claim 15]

The semiconductor memory device according to Claim 13 or Claim 14, wherein said barrier metal layer is a first titanium nitride layer and said refractory metal layer is a first tungsten layer.

[Claim 16]

The semiconductor memory device according to any of Claims 13 to 15, wherein each of said first capacitor section and said second capacitor section extends from a surface to inside of said first insulating film to have a trench structure.

[Claim 17]

The semiconductor memory device according to any of Claims 13 to 16, wherein said first capacitor section is formed perpendicularly above said first source region, and said second capacitor section is formed perpendicularly above said second source region.

[Claim 18]

The semiconductor memory device according to any of Claims 13 to 17, wherein each of said first bottom electrode and said second bottom electrode has a laminate structure of a titanium nitride layer and a doped polysilicon layer.

[Claim 19]

The semiconductor memory device according to any of Claims 13 to 18, wherein each of said first upper electrode and said second upper electrode has a laminate structure of a titanium nitride layer and a doped polysilicon layer.

[Claim 20]

The semiconductor memory device according to any of Claims 13 to 19, wherein each of said first dielectric layer and said second dielectric layer is formed with high dielectric constant material.

[Claim 21]

The semiconductor memory device according to any of Claims 13 to 20, further comprising a third contact portion [which is] formed in upper perpendicular direction from said drain region through said first insulating film to include a second metal plug portion.

[Claim 22]

The semiconductor memory device according to Claim 21, wherein said second metal plug portion includes a second titanium nitride layer formed within side and bottom portions thereof, a second tungsten layer formed inside said second titanium nitride layer.

[Claim 23]

The semiconductor memory device according to any of Claims 13 to 22, further comprising:

a second insulating film covering said first capacitor section, said second capacitor section, and said first insulating film; and

a fourth contact portion which extends from a surface of said second insulating film to said third contact portion through said first insulating film.

[Claim 24]

The semiconductor memory device according to Claim 23, wherein said third contact portion and said fourth contact portion work as a bit line.

[Claim 25]

A manufacturing method of a semiconductor device comprising:

(a) a step of forming a MOS transistor which includes a gate, a source region, and a drain region in a surface portion of the semiconductor substrate;

(b) a step of forming a first insulating film covering said MOS transistor:

(c) a step of forming a first contact portion connected with said source region and a second contact portion connected with said drain region through said first insulating film;

(d) a step of forming a second insulating film on said first insulating film, said first contact portion, and said second contact portion;

(e) a step of forming a capacitor section extending from a surface of said second insulating film to said first contact portion to be connected with said first contact portion.

[Claim 26]

The manufacturing method of the semiconductor device

according to Claim 25, wherein said step (c) further includes:

(f) a step of opening a first contact hole extending from a surface of said first insulating film to said source region, and a second contact hole extending from a surface of said first insulating film to said drain region at the same time;

(g) a step of forming barrier metal layers on respective sides of said first and second contact holes at the same time;

(h) a step of forming refractory metal layers on said barrier metal layers, respectively, within said first and second contact holes at the same time.

[Claim 27]

The manufacturing method of the semiconductor device according to Claim 25 or Claim 26, wherein said step (e) further includes:

(i) a step of forming an opening extending from a surface of said second insulating film to said first contact portion;

(j) a step of forming a bottom electrode on a side and bottom of said opening;

(k) a step of forming a dielectric layer on said bottom electrode; and

(l) a step of forming a upper electrode on said dielectric layer.

[Claim 28]

The manufacturing method of the semiconductor device

according to Claim 27, wherein said second insulating film includes a third insulating film and a fourth insulating film, and said step (i) includes:

(m) a step of forming said third insulating film which covers said first insulating film, said first contact portion, a said second contact portion;

(n) a step of forming said fourth insulating film on said third insulating film;

(o) a step of forming an opening extending from a surface of said fourth insulating film to a surface of said third insulating film perpendicularly above said first contact portion by an etching technique;

(p) a step of etching said third insulating film to form said opening reaching said first contact portion.

[Claim 29]

The manufacturing method of the semiconductor device according to Claim 28 wherein, said third insulating film functions as an etching stopper.

[Claim 30]

The manufacturing method of the semiconductor device according to any of Claims 25 to 29 further comprising:

(q) a step of forming a fifth insulating film which covers said capacitor section and said second insulating film;

(r) a step of forming a third contact portion which extends from a surface of said fifth insulating film to said second contact portion at said second insulating film.

[Claim 31]

The manufacturing method of the semiconductor device according to any of Claims 25 to 30, wherein a logic section transistor having a gate, a source region, and a drain region is formed in said surface portion of said semiconductor substrate of said semiconductor memory device for a peripheral logic section, and

wherein said logic section transistor is covered with said first insulating film, and said method further comprising:

(s) a step of forming said first contact portion, said second contact portion, a first source contact portion connected with a source region of said peripheral logic section, and a first drain contact portion connected with a drain region of said peripheral logic section through said first insulating film at the same time.

[Claim 32]

The manufacturing method of the semiconductor device according to Claim 31, further comprising:

(t) a step of forming a sixth insulating film covering said first insulating film, said first source contact portion and said second drain contact portion;

(u) a step of forming said third contact portion, a second source contact portion extending from a surface of said sixth insulating film to said first source contact portion in said sixth insulating film, and a second drain contact portion extending from a surface of said sixth insulating film to said first drain contact portion through said sixth insulating film at the same time.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention belongs]

The present invention is related to a semiconductor memory device (DRAM), especially, related to a structure of the semiconductor memory device and a manufacturing method of the same.

[0002]

[Conventional Technique]

A memory cell of DRAM of a semiconductor memory device is generally constituted by a capacitor and a transistor.

[0003]

Fig. 16 is a cross-section view illustrating a structure of a conventional semiconductor memory device.

[0004]

As shown in Fig. 16, a diffusion layer region is formed in a surface portion of a P-type silicon substrate 100. STI oxide films 101, LDDs (lightly doped drain) 111, LDDs 111', and N-type source diffusion layers 113 are formed in pairs in the surface portion of the P-type silicon substrate 100. The STI oxide films 101 are used to electrically insulate the adjacent diffusion layer regions. It should be noted that the LDDs 111 and 111' are formed in a single process. The STI oxide films 101 and the source diffusion layers 113 are connected each other. The LDDs 111 and the source diffusion layers 113 are connected each other.

Insulating films 132 are formed on the surfaces of the source diffusion layers 113. Also, an N-type drain diffusion layer 114 is formed in the surface portion of the P-type silicon substrate 100. One of the above mentioned LDDs 111' and the drain diffusion layer 114 are connected each other. The other of the LDDs 111' and the drain diffusion layer 114 are connected each other. An insulating films 132' is formed on the surfaces of the drain diffusion layer 114. It should be noted that the insulating films 132 and the insulating film 132' are formed in a single process. Direct nitride films 115 are formed on the surfaces of the STI oxide films 101 and the insulating films 132.

[0005]

Gate oxide films 110 are formed on the surface of the P-type silicon substrate 100. Gates 103 as word lines are formed on the surfaces of the gate oxide films 110. The insulating films 133 are formed on the surfaces of the gates 103. Sidewalls 112 are formed on the surfaces of the LDDs 111 and 111'. The sidewalls 112 are connected with the LDDs 111 and 111', the gates 103, and the insulating films. Direct nitride films 115' are formed on the surfaces of the insulating films 132, the sidewalls 112, the insulating films 133, and the insulating film 132'. It should be noted that the direct nitride films 115 and 115' are formed in a single process. Thus, MOS transistors are formed on or in the surface portion of the P-type silicon substrate 100. Also, a buried oxide film 116 covering the above mentioned MOS transistors are formed on the surfaces of the direct

nitride films 115 and 115'.

[0006]

Capacitor contacts 104 are formed on the surfaces of the source diffusion layers 113 to extend to the surface of the buried oxide film 116 in the perpendicular direction. The capacitor contacts 104 are formed with polysilicon layers 105. An oxide film 122 is formed on the surface of the buried oxide film 116. Bottom electrodes are formed perpendicularly on the capacitor contact 104 in the upper side of capacitor contact 104 to consist of bottom and side portions, the side portion extending upward from the edge of the bottom portion to the surface of the oxide film 122. These bottom electrodes are formed with polysilicon layers 106. Ta_2O_5 capacitor films 107 are formed as dielectric layers on the surfaces of the bottom electrodes (polysilicon) 106 and the oxide film 122. Upper electrodes are formed on the surfaces of the Ta_2O_5 capacitor films 107. These upper electrodes consist of titanium nitride layers 108 formed on the surfaces of the Ta_2O_5 capacitor film 107 and polysilicon layers 109 formed on the surfaces of the titanium nitride layers 108. As thus described, capacitor sections are formed with the upper electrodes, the dielectric layers, and the bottom electrodes on the top of the capacitor contact 104. Additionally, an oxide film 135 is formed on the oxide film 122 and the capacitor sections to cover the capacitor sections.

[0007]

A bit contact 102 is formed on the surface of the

drain diffusion layer 114 to reach the surface of the oxide film 135 in the perpendicular direction through the buried oxide film 116, the oxide film 122 and the oxide film 135. The bit contact 102 divides the above mentioned diffusion layer region into two memory cell regions. The bit contact 102 is plugged with tungsten. Additionally, a bit line 131 is connected with the top of the bit contact 102 to extend along the surface of the oxide film 135. The bit line 131 is formed with titanium nitride. It should be noted that the bit contact 102 functions as a bit line to provide a connection to the bit line 131.

[0008]

Thus, the diffusion layer region is formed in the surface portion of the P-type silicon substrate 100. This diffusion layer region is electrically insulated from the adjacent diffusion layer region by the STI oxide films 101. The diffusion layer region is divided into two memory cell regions by the single bit contact 102. In the cross section of the conventional semiconductor memory device, the gates 103 as word lines are positioned on the both sides of the bit contact 102 in the diffusion layer region. Additionally, the conventional semiconductor memory device has the capacitor contacts 104 to be connected with the capacitor sections across the gates 103 with the bit contact 102 centered. In other words, in the conventional semiconductor memory device, the single bit contact 102, the pairs of the gates 103, and the capacitor contacts 104 are disposed in one diffusion layer region so as to form two memory cell

sections. Next, the capacitor sections have the capacitor contacts 104 formed with the polysilicon layers 105, and the bottom electrodes formed with the polysilicon layers 106, the capacitor dielectric films formed with the Ta_2O_5 107, and the upper electrodes formed by the titanium nitride layers 108 and the polysilicon layers 109. The upper electrodes (the titanium nitride layers 108, the polysilicon layers 109) are called as "plate" and kept having the same potential for all of the memory cells.

[0009]

Next, the above-mentioned manufacturing method of the semiconductor memory device is described bellow with reference to Fig 16.

[0010]

Showing the forming method simply, first of all, STI oxide films 101 are formed on the P-type silicon substrate 100. A well is formed in a diffusion layer region by an ion implantation. Then, gate oxide films 110 and polysilicon layers for gates 103 are successively formed on the formed well. Sidewalls 112 are formed on both sides of the gates 103. Source diffusion layers 113 and a drain diffusion layer 114 are formed in the diffusion layer region except the gates 103 and the sidewalls 112 by an ion implantation. Next, the gates 103, the source diffusion layers 113, the drain diffusion layer 114 are subjected to a cobalt silicide process. Then, insulating films 133 are formed on the surface of the gate 103, insulating films 132 are formed on the surface of the source diffusion layers 113, and an

insulating film 132' is formed on the surface of the drain diffusion layer 114.

[0011]

Next, capacitor contacts 104 are formed on the surfaces of the source diffusion layers 113 to provide connections with capacitor sections. The capacitor contacts 104 are embedded with the polysilicon layer 105. Direct nitride films 115 are formed on the surfaces of the STI oxide films 101 and the insulating films 132. Direct nitride films 115' are formed on the surfaces of the insulating films 132, the sidewalls 112, the insulating films 133, and the insulating film 132'. Moreover, a buried oxide film 116 is formed on the surfaces of the direct nitride films 115 and the direct nitride film 115'. An oxide film 122 is formed on the surface of the buried oxide film 116. The buried oxide film 116 over the capacitor contacts 104 are partially removed, and polysilicon layers 106 for the bottom electrodes are formed on the top of the capacitor contacts 104. The bottom electrodes (the polysilicon layer) 106 are formed through subjecting the surfaces of these polysilicon layers 106 to an HSG process and an etchback process. After that, Ta_2O_5 capacitor films 107 as the dielectric layers are formed on the bottom electrodes (the polysilicon layers) 106 and on the partial surface of the oxide film 122. Titanium nitride layers 108 and polysilicon layers 109 are laminated as the upper electrodes on the Ta_2O_5 capacitor films 107. The capacitor sections are constituted with the bottom electrodes, the dielectric layers and the upper electrodes.

Also, an oxide film 122 and an oxide film 135 covering the capacitor sections are formed on the surface of the oxide film 122 and the capacitor sections.

[0012]

Next, a bit contact 102 is formed on the surface of the drain diffusion layer 114 to reach the surface of the oxide film 135 in the perpendicular direction through the buried oxide film 116, the oxide film 122, and the oxide film 135. The bit contact 102 is embedded with tungsten. A bit line 131 is formed on the upper side of the bit contact 102 to extend in the direction along the surface of the oxide film 135. Memory cells are formed by such method for the conventional semiconductor memory device.

[0013]

Electrical operations of the conventional semiconductor memory device involve transfer of electrical charges accumulated in the capacitor sections through the bottom electrodes (the polysilicon layer) 106, the capacitor contacts 104, the source diffusion layers 113 of the transistors, the channels, the drain diffusion layer 114, the bit contact 102, and the bit line 131 in series. However, in the conventional semiconductor memory device, a high-speed operation owes the resistance in the paths of the electric charges, and especially the speed is restricted by the high resistance part. Recently, the conventional semiconductor memory device suffers from problems caused by high contact resistance between the capacitor contacts 104 and the source diffusion layers 113, high resistance of the

capacitor contacts 104 resulting from the polysilicon layers 105, and high resistance in the bottom electrodes 106 resulting from the polysilicon. Therefore, reducing the resistance of the above mentioned path is required for high-speed operations; especially, replacing the capacitor contact portions 104 formed with polysilicon with metal contacts, and thereby reducing the resistance of the bottom electrode 106 are required.

[0014]

Additionally, as shown in Fig. 16, the bit contact 102 experiences difficulty with being etched because it requires forming high aspect ratio openings after forming the capacitor sections.

[0015]

Also, in the domestic re-publication of PCT international publication WO098/028795, a semiconductor memory device including memory cells and its circumference circuit for high integration and high reliability is disclosed. This semiconductor memory device, which has a memory cell region including a first transistor provided for a main surface of a semiconductor substrate, and a logic circuit region including a second and third transistors whose conductivity types are different from each other, is characterized in that a first interconnection of a first metal is formed on the main surface of a first insulating film provided on the first, second and third transistors for the memory cell region and the logic circuit region, respectively, and the connections of the first

interconnection with the first, second, and third transistors are achieved by a connection body including a first body formed inside an opening which penetrates the first insulating film.

[0016]

Further, in Japanese Laid Open Patent Application (JP 2000-114475), an invention titled "stacked capacitor memory cell and manufacturing method of the same" is disclosed for resolving a difficulty in the forming process of small-sized and high-density capacitors for memory cells including a field effect transistor and a stacked capacitor. This invention titled "stacked capacitor memory cell and manufacturing method of the same", which addresses a memory cell including a semiconductor body and a capacitor, is characterized in that the semiconductor body includes first and second regions of one of conductivity types in a partial surface portion thereof, the regions being separated by an intermediate region of another conductivity type to form a transistor, and that the capacitor, which is formed on the first region, includes a conductive plug providing an electric connection with the first region, a conductive layer providing a diffusion barrier on the plug, a dielectric layer member provided to cover the plug on the barrier layer, a first metal layer formed at least on the side of the dielectric layer member and electrically connected to the diffusion barrier to function as an inside electrode of the capacitor, and a second metal layer provided on the top and side surfaces of the dielectric

layer member to function as an outside electrode of the capacitor.

[0017]

Furthermore, in Japanese Laid Open Patent Application (JP 2000-156479), " The semiconductor memory device and the manufacturing method of the same." is disclosed, wherein the device has a cylinder-type capacitor in a MIM structure and a capacitor loss and a junction leak caused by the sticking layer or the barrier layer at the electrode sidewall are prevented, and a reaction between a silicon and an electrode material is prevented. This semiconductor memory device and manufacturing method of the same include; a semiconductor substrate on which an active element was formed; an interlayer insulating film formed on the semiconductor substrate; a contact hole reaching the surface of the active element and provided for the interlayer insulating film; a plug of conductive body formed in the contact hole; a barrier layer formed to cover the upper side of the plug at least on the surface of the interlayer insulating film; a bottom formed on upper side of the barrier layer; a bottom electrode having a trench structure of the lateral side formed from the end of the bottom in the upper direction; a capacitor insulating of dielectric formed on the surface of the bottom electrode; and upper electrode formed on the surface of the capacitor insulating film

[0018]

Moreover, in the invention of Japanese Laid Open Patent Application (JP H11-214644), " The semiconductor

integrated circuit and the manufacturing method of the same." is disclosed. In this semiconductor integrated circuit and the manufacturing method of the same, an extended interconnection is formed so as to contact with the first insulating film at least in one part of the wiring line on the first insulating film of the silicon oxide which is formed on the main surface of the semiconductor substrate. A capacitor element including a capacitor insulating film, which is formed by high dielectric constant material at least in one part, is formed on the second insulating film which was formed on the wiring line. A conductive film including the wiring line is formed by a refractory metal excluded titanium or a nitride of the refractory metal at least in a part contact with the surface of the first insulating film.

[0019]

[Problems the Invention Tries to Solve]

There is a problem that the resistance between the source portions (the source diffusion layer) of cell transistors and contact portions to achieve a connection with the electrodes of the capacitor sections is large for achieving high-speed operation of DRAMs. This mainly results from the use of polysilicon plugs for contact portions. Specifically, the resistance includes the contact resistance between the cobalt silicide source portions and contact polysilicon plugs and the resistance of the contact polysilicon plugs by themselves, and so on.

[0020]

Another problem is the difficulty in the etching process, which results from that the bit contact requires forming the contact hole having an increased aspect ratio deeper than a total height of the cylinder capacitor sections and the capacitor contact portions.

[0021]

An object of the present invention is to provide a semiconductor memory device and a manufacturing method of the same for reducing the electric power consumption and achieving the high-speed operation.

[0022]

Another object of the present invention is to provide a semiconductor memory device and a manufacturing method of the same for improving a productivity by opening through holes for capacitor contact portions and bit contact portions at the same time.

[0023]

Still another object of the present invention is to provide a semiconductor memory device and a manufacturing method of the same for reducing an aspect ratio of a bit contact etching to facilitate the etching process.

[Means for Solving the Problems]

[0024]

A means for solving the problems is now described bellow. The technical terms in the description have numbers and symbols with parentheses "( )". The numbers and symbols correspond to the technical term in at least one of the embodiments of the present invention, particularly they

coincide with the reference numbers and symbols for the technical terms described in the drawings of the embodiment. These numbers and symbols clarify the correspondence between the technical article in the Claims and the technical article in the embodiment. These correspondences do not mean that the technical articles in the claims are interpreted with the limitation to the technical articles in the embodiments.

[0025]

The semiconductor memory device of the present invention comprises a MOS transistor formed on a surface of a semiconductor substrate (50), wherein the MOS transistor has a gate (10), a source region (13), a drain region (14); comprises a first insulating film (16,21,22) to cover the MOS transistor; comprising a capacitor formed on the first insulating film (16, 21, 22), wherein the capacitor includes a bottom electrode (6), a dielectric layer formed on the bottom electrode(6), an upper electrode (8) formed on the dielectric layer; and comprises a first contact portion (17') formed in the first insulating film (16, 21, 22) extending from the bottom electrode (6) to the source region (13). The first contact portion (17') includes a first metal plug portion.

[0026]

Also, the first metal plug portion includes a barrier metal layer formed within side and bottom portions a refractory metal layer formed inside the barrier metal layer. The barrier metal layer is a first titanium nitride layer

(19) and the refractory metal layer is a first tungsten layer (20).

[0027]

Also, the capacitor section is formed to be extended from the surface of the first insulating film (16, 21, 22) to the inside of the first insulating film (16, 21, 22) to have trench structure and is formed in an upper perpendicular direction. The bottom electrode (6) is a laminate structure of a titanium nitride layer (23) and a doped polysilicon layer (25). the upper electrode (8)is a laminate structure in the titanium nitride layer (28) and the doped polysilicon layer (29).

the dielectric layer is high dielectric constant material (27).

[0028]

The semiconductor memory device of the present invention further includes a second contact portion (18') which is formed in the upper perpendicular direction from the drain region (14) at the first insulating film (16, 21, 22) and includes a second metal plug portion.

[0029]

Also, the second metal plug portion includes the second titanium nitride layer (19) which is formed on a sidewall periphery and a bottom, and includes the second tungsten layer (20) which is formed in the second titanium nitride layer (19).

[0030]

The semiconductor memory device of the present

invention further includes a second insulating film (35) which covers the capacitor section and the first insulating film (16,21,22), and a third contact portion (30) which extends from the surface of the second insulating film (35) to the second contact portion (18') at the first insulating film. The second contact portion (18') and the third contact portion (30) work as a bit line.

[0031]

The semiconductor memory device of the present invention further comprises a first MOS transistor formed on a first surface of a semiconductor substrate (50), wherein the first MOS transistor has a first gate (10), a first source region (13), a drain region (14); includes a second MOS transistor formed on a second surface of the semiconductor substrate (50), wherein the second MOS transistor has a second gate (10), a second source region (13), the drain region (14), in which the drain region (14) is shared with the first MOS transistor and the second MOS transistor; and includes a first insulating film (16,21,22) covering the first MOS transistor and the second MOS transistor, a first capacitor formed on the first insulating film to have a trench structure, wherein the first capacitor includes a first bottom electrode (6), a first dielectric layer formed on the first bottom electrode (6) and a first upper electrode (8) formed on the first dielectric layer; a second capacitor formed on the first insulating film (16, 21, 22) to have trench structure, wherein the second capacitor includes a second bottom

electrode(6), a second dielectric layer formed on the second bottom electrode(6) and a second upper electrode (8) formed on the second dielectric layer; and a first contact portion (17') which is formed on the first insulating film (16,21,22) extending from the first bottom electrode(6) to the first source region(13) and a second contact portion(17') which is formed on the first insulating film (16,21,22) extending from the second bottom electrode (6) to the second source region(13). The each of the first contact portion (17') and the second contact portion (17') includes a first metal plug portion.

[0032]

Also, the first metal plug portion includes a barrier metal layer formed on a sidewall periphery and a bottom and includes a refractory metal layer formed on the barrier metal layer. The barrier metal layer is a first titanium nitride layer (19) and the refractory metal layer is a first tungsten layer(20).

[0033]

Also, each of the first capacitor section and the second capacitor section extends from a surface of the first insulating film (16,21,22) into the first insulating film (16,21,22) to have trench structure. The first capacitor section is formed perpendicularly above the first source region (13) and the second capacitor section is formed perpendicularly above the second source region (13). Each of the first bottom electrode (6) and the second bottom electrode (6) has a laminate structure of a titanium nitride

layer (23) and a doped polysilicon layer (25). Each of the first upper electrode (8) and the second upper electrode has a laminate structure of a titanium nitride layer (28) and a doped polysilicon layer (29). Each of the first dielectric layer and the second dielectric layer is high dielectric constant material (27).

[0034]

The semiconductor memory device of the present invention further comprises a third contact portion (18') which is formed in upper perpendicular direction from the drain region (14) at the first insulating film(16,21,22) including a second metal plug portion.

[0035]

Also, the second metal plug portion includes a second titanium nitride layer (19) formed within side and bottom portions, and a second tungsten layer formed inside the second titanium nitride layer (19).

[0036]

The semiconductor memory device of the present invention further comprises a second insulating film (35) covering the first capacitor section, the second capacitor section and the first insulating film (16,21,22); and a fourth contact portion (30) which extends from a surface of the second insulating film (35) to the third contact portion (18') at the first insulating film (16,21,22).
The third contact portion (18') and the fourth contact portion (30) work as a bit line.

[0037]

A manufacturing method of a semiconductor device according to the present invention comprises: (a) a step of forming a MOS transistor which includes a gate (10), a source region (13), and a drain region (14) on a surface of the semiconductor substrate(50); (b) a step of forming a first insulating film (16) which covering the MOS transistor: (c) a step of forming a first contact portion (17') connected with the source region (13) and a second contact portion (18') connected with the drain region(14) on the first insulating film (16); (d) a step of forming a second insulating film (21,22) on the first insulating film (16), the first contact portion (17'), and the second contact portion (18'); (e) a step of forming a capacitor section which is extended from a surface of the second insulating film (21,22) to the first contact portion (17') and is connected with the first contact portion (17').

[0038]

In the manufacturing method of the semiconductor device according to the present invention, the step (c) further includes: (f) a step of opening a first contact hole (17) extending from a surface of the first insulating film (16) to the source region (13) and a second contact hole (18) extending from a surface of the first insulating film (16) to the drain region (14) at the same time; (g) a step of forming a barrier metal layer on each sidewall periphery of the first contact hole (17) and the second contact hole (18) at the same time; (h) a step of forming a refractory metal layer on each the barrier metal layer of the first

contact hole (17) and the second contact hole (18) at the same time.

[0039]

In the manufacturing method of the semiconductor device according the present invention, the step (e) further includes: (i) a step of forming an opening extending from a surface of the second insulating film (21,22) to the first contact portion (17'); (j) a step of forming a bottom electrode (6) on the sidewall periphery and a bottom of the opening; (k) a step of forming a dielectric layer on the bottom electrode (6): (l) a step of forming a upper electrode (8) on the dielectric layer.

[0040]

In the manufacturing method of the semiconductor device according to the present invention, the second insulating film (21,22) includes a third insulating film (21) and a fourth insulating film (22): and the step (i) includes (m) a step of forming the third insulating film (21) which covers the first insulating film (16), the first contact portion (17'), a the second contact portion (18'); (n) a step of forming the fourth insulating film (22) on the third insulating film (21); (o) a step of forming an opening by an etching perpendicularly above the first contact portion (17') from a surface of the fourth insulating film (22) to a surface of the third insulating film (21); (p)a step of etching the third insulating film (21)to form the opening reaching the first contact portion (17'). The third insulating film works as an etching stopper.

[0041]

The manufacturing method of the semiconductor device according the present invention further comprises (q) a step of forming fifth insulating film (35) which covers the capacitor section and the second insulating film (21,22); (r) a step of forming a third contact portion (30) which extends from a surface of the fifth insulating film (35) to the second contact portion (18') at the second insulating film (21,22).

[0042]

In the manufacturing method of the semiconductor device according to the present invention, a logic section transistor which has a gate (10) of a peripheral logic section, a source region (13), a drain region (14) is formed on the surface of the semiconductor substrate (50) of the semiconductor memory device and the logic section transistor is covered with the first insulating film (16). The manufacturing method of the semiconductor device according to the present invention further comprises (s) a step of forming the first contact portion (17'), the second contact portion (18'), the first source contact portion (17') connected with a source region (13) of the peripheral logic section, and a first drain contact portion (18') connected with a drain region (14) of the peripheral logic section on the first insulating film (16) at the same time.

[0043]

The manufacturing method of the semiconductor device according to the present invention further comprises (t) a

step of forming a sixth insulating film (62) covering the first insulating film (16), the first source contact portion (17') and the second drain contact portion (18'); and (u) a step of forming the third contact portion (30), a second source contact portion (63) extending from a surface of the sixth insulating film (62) to the first source contact portion (17') in the sixth insulating film (62), and a second drain contact portion (60) extending from a surface of the sixth insulating film (62) to the first drain contact portion (18') in the sixth insulating film (62) at the same time.

[0044]

In the semiconductor memory device according to the present invention, the contact resistance and the resistance of the first contact portion (17') and the second contact portion (18') can be lowered by that the first contact portion (17') and the second contact portion (18') are opened at the same time, and are replaced into the metal plug portion.

[0045]

Also, the titanium nitride layer (23) does not only work as the barrier metal which can prevent the metallic plug portion (the first contact portion (17')) and doped polysilicon layer (25) from reacting directly but also a low resistance electrode can be formed by forming the bottom electrode (6) in the multiple structure of the titanium nitride layer (23) and the DOPOS layer (25).

As a result, in the semiconductor memory device according to

the present invention, a low voltage and high-speed operation can be possible.

[0046]

Also in the manufacturing method of the semiconductor memory device according to the present invention, the aspect ratio of the bit contact etching can be small and a manufacture by the etching can be facilitated by forming the third contact portion (30) on the second contact portion (18').

[0047]

[Embodiments of the Invention]

Embodiments of a semiconductor memory device according to the present invention will be described below with reference to the attached drawings.

[0048]

(Embodiment 1)

Fig. 1 is a cross-section diagram showing a structure of a semiconductor memory device according to the embodiment 1 of the present invention.

[0049]

As shown in Fig. 1, a diffusion layer region is formed in the surface portion of a P-type silicon substrate 50. STI oxide films 1, LDDs (lightly doped drain) 11, LDDs 11', N-type source diffusion layers 13 are formed on the surface of the P-type silicon substrate 50 in pairs. The STI oxide films 1 are used for electrically insulating the adjacent diffusion layer regions. It should be noted that LDDs 11 and 11' are formed in a single process. The STI

oxide films 1 and the source diffusion layers 13 are connected each other. The LDDs 11 and the source diffusion layers 13 are connected each other. Insulating films 32 are formed on the surfaces of the source diffusion layers 13. Also, an N-type drain diffusion layer 14 is formed in the surface portion of the P-type silicon substrate 50. One of the aforementioned LDDs 11' and the drain diffusion layer 14 are connected each other. Also, the other LDD 11' and the drain diffusion layer 14 are connected each other. An insulating film 32' is formed on the surface of the drain diffusion layer 14. It should be noted that the insulating films 32 and 32' are formed in a single process. Direct nitride films 15 are formed on the surface of the STI oxide films 1 and the insulating films 32.

[0050]

Gate oxide films 9 are formed on the P-type silicon substrate 50. Gates 10 used as word lines are formed on the surfaces of the gate oxide films 9. Insulating films 33 are formed on the surfaces of the gates 10. Sidewalls 12 are formed on the surface of LDDs 11 and 11'. The sidewalls 12 are connected with the LDDs 11 and 11', the gates 10, and the insulating films 33. Direct nitride films 15' are formed on the sidewalls 12, the insulating films 33, the insulating film 32'. It should be noted that the direct nitride films 15 and 15' are formed in a single process. MOS transistors are herewith formed in the surface portion of the P-type silicon substrate 50. A buried oxide film 16 covering the aforementioned MOS transistor is formed on the

surface of direct nitride films 15 and 15'.

[0051]

Contact portion metal plugs 17' are formed on the source diffusion layers 13 to extend to the surface of the buried oxide film layer 16 in the perpendicular direction. A contact portion metal plug 18' is formed on the surface of the drain diffusion layer 14 to extend to the surface of the buried oxide film 16 in the perpendicular direction. The contact portion metal plugs 17' and the contact portion metal plug 18' are composed of a titanium nitride layer 19 as a barrier metal layer, a tungsten layer 20 of refractory metal. A stopper silicon oxynitride film 21 is formed on the surface of the buried oxide film 16. An interlayer plasma oxide film 22 is formed on the surface of the silicon oxynitride film 21.

[0052]

Bottom electrodes 6 are formed perpendicularly on the contact portion metal plugs 17' to include bottom and side portions, the side portion being formed to extend upward from the edge of the bottom portion to the surface of the interlayer plasma oxide film 22. The bottom electrodes 6 are formed with a stack of a titanium nitride layer 23 and a DOPOS (doped polysilicon) layer 25, the titanium nitride layer 23 being formed from the bottom portion to the middle of the side portion, and the DOPOS layer 25 being formed within the side and bottom portions. Ta_2O_5 capacitor films 27 of high dielectric constant material are formed as dielectric layers on the bottom electrode 6 and on the

surface of a portion of the interlayer plasma oxide film 22. Upper electrodes 8 are formed on the surface of the Ta_2O_5 capacitor films 27. The upper electrodes 8 are formed with a stack of a titanium nitride layer 28 formed on the surface of Ta_2O_5 capacitor film 27 and a DOPOS (doped polysilicon) layer 29 formed on the surface of the titanium nitride layer 28. As described, trench-structured capacitor sections, which are comprised of the upper electrodes 8, the dielectric layers (the Ta_2O_5 capacitor film 27), and the bottom electrodes 6, are formed on the contact portion metal plugs 17'. Additionally, an oxide film 35 is formed on the surface of the interlayer plasma oxide film 22 and the capacitor sections to cover the interlayer plasma oxide film 22 and the capacitor sections.

[0053]

Additionally, a bit contact 30 is formed on the contact portion metal plug 18' to extend from the surface of the oxide film 35 to the contact portion metal plug 18' through the silicon oxynitride film 21, the interlayer plasma oxide film 22 and the oxide film 35. The above mentioned diffusion layer region is divided into two memory cell regions by the bit contact 30. The bit contact 30 is plugged with tungsten. Also, a bit line 31 is connected with the upper portion of the bit contact 30 to extend along the surface of the oxide film 35. The bit line 31 is formed with titanium nitride. Also, the bit contact 30 functions as a bit line to provide connections to the bit line 31.

[0054]

In this way, the semiconductor memory device according to the embodiment 1 reduces contact resistances of the contacts and resistances of the contact plugs through forming the contact plugs of the capacitor contact portions (the capacitor contact 17) and the bit contact portion (the cell contact 18) with metal plugs (the contact portion metal plugs 17', and the contact portion metal plug 18'). Additionally, in the semiconductor memory according to the embodiment 1, the bottom electrodes 6, which is formed with the dual-layer structure of the titanium nitride layer 23 and the DOPOS layer 25, functions as barrier metal for preventing direct reaction of the contact portion metal plug 17' and the DOPOS layer 25, and also provides low resistance electrodes. Furthermore, the semiconductor memory according to the embodiment 1 reduces the aspect ratio of bit contact etching through providing the cell contact 18 below the bit contact 30.

[0055]

Next, a manufacturing process of the aforementioned semiconductor memory device according to the embodiment 1 is described with reference to Fig. 2 to Fig.12.

[0056]

Fig. 2 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0057]

Fig. 3 is a cross-section view illustrating the

manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0058]

Fig. 4 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0059]

Fig. 5 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0060]

Fig. 6 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0061]

Fig. 7 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0062]

Fig. 8 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0063]

Fig. 9 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0064]

Fig. 10 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0065]

Fig. 11 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0066]

Fig. 12 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[0067]

As shown in Fig. 2, STI oxide films 1 of 3500 Å in depth for isolation are formed on a P-type silicon substrate 50. After that, a well is formed through an ion implantation into the surface portion of the P-type silicon substrate 50. After forming gate oxide films 9 of 70 Å in thickness, DOPOS of 1500 Å in thickness is then deposited, and the gate 10 is then formed through lithography and

plasma etching processes. LDDs 11 are formed through an implantation in the surface portion of the P-type silicon substrate 50. After forming the LDDs 11 through the implantation, sidewalls 12 are formed on the surfaces of the LDDs 11. Additionally, source diffusion layers 13 and drain diffusion layer 14 are formed through an ion implantation in the surface portion of the P-type silicon substrate 50. After that, the gate 10, the source diffusion layers 13, and the drain diffusion layers 14 are subjected to a cobalt silicide process. Additionally, insulating films 33 are formed on the gates 10, insulating films 32 are formed on the source diffusion layers 13, and the insulating film 32' is formed on the drain diffusion layer 14.

[0068]

Next, as shown in Fig. 3, the surfaces of the STI oxide films 1 and the insulating films 32 are covered with direct nitride films 15. The surfaces of the insulating films 32, the sidewalls 12, the insulating films 33, the insulating film 32' are covered with the direct nitride film 15' of 400 Å in thickness. Moreover, the surfaces of the direct nitride films 15 and the direct nitride film 15' are covered with an oxide film 16 of 6000 Å in thickness. Contact holes are formed at the same time to expose both of the source diffusion layers 13 and the drain diffusion layer 14. In other words, capacitor contact holes 17 and a cell contact hole 18 are formed at the same time, the capacitor contact holes 17 extending upward to expose the source diffusion layers 13, and a cell contact hole 18 extending

upward to expose the drain diffusion layer 14.

[0069]

Next, as shown in Fig. 4, a titanium nitride layer 19 to be barrier metal layers is deposited on the side and bottom portions of the capacitor contact holes 17, and the cell contact hole 18. A refractory metal tungsten layer 20 is embedded inside the titanium nitride layer 19, which is formed on both of the capacitor contact holes 17 and the cell contact hole 18. Additionally, as shown in Fig. 5, after deposition of the titanium nitride layer 19 and the tungsten layer 20, a tungsten etchback or a CMP process are implemented to form contact portion metal plugs 17' with the titanium nitride layer 19 and the tungsten layer 20 inside the capacitor contact holes 17, and to form a contact portion metal plug 18' with the titanium nitride layer 19 and the tungsten layer 20.

[0070]

Next, as shown in Fig. 6, a silicon oxynitride film 21 of 500 Å in thickness is deposited on the surface of the buried oxide film 16, the contact portion metal plug 17' and the contact portion metal plug 18'. After the deposition of the silicon oxynitride film 21, a cylinder interlayer film is formed with a plasma oxide film 22 of 10000 Å in thickness on the surface of the silicon oxynitride film 21. The cylinder interlayer film (the plasma oxide film 22) is subjected to lithography and dry etching techniques to form openings through etching downward from the surface thereof to the surface of the silicon oxynitride film 21, which

functions as an etching stopper, toward the contact portion metal plugs 17 in the perpendicular direction. In order to remove the silicon oxynitride film 21 for the stoppers, this etching is achieved for the openings to reach the contact portion metal plugs 17', and to provide openings 34.

[0071]

Next, as shown in Fig. 7, the side portions of the openings 34 are covered with a titanium nitride layer 23 of 100 Å in thickness for providing the bottom electrodes 6, and resist material 24 is then left only inside of the cylinders. As shown in Fig. 8, the titanium nitride layer 23 is formed only inside the cylinders within the openings 34 through a etchback technique using dry etching.

[0072]

Next, as shown in Fig. 9, after removing the resist material 24, DOPOS layers 25 of 550 Å in thickness are deposited on the side surfaces of the openings 34, which are covered with the titanium nitride layer 23. The surfaces of the openings 34 covered with the DOPOS layers 25 are subjected to a HSG process. Then, resist material 26 is left only inside of the cylinders on the HSG-processed surfaces of the openings 34. The HSG-processed DOPOS layers 25 are formed through an etchback technique with a dry etching process only inside the cylinder of the openings 34, in which the resist material 26 is disposed. The titanium nitride layer 23 should be formed to have a reduced height through the preceding processes so as not to be exposed.

After that, as shown in Fig.10, the bottom electrodes 6 are completed by removing the resist material 26 in the cylinders of the openings 34, where the DOPOS layers 25 are formed.

[0073]

As shown in Fig. 11, Ta_2O_5 capacitor films 27 of high dielectric constant material of 80 Å in thickness are then deposited on the surfaces of the bottom electrodes 6 as dielectric layers. Titanium nitride layers 28 of 100 Å in thickness and DOPOS 29 of 1500 Å in thickness are deposited on the surfaces of the Ta_2O_5 capacitor films 27 to provide the upper electrodes 8. This completes the aforementioned capacitor sections. An oxide film 35 is formed on the surface of the interlayer plasma oxide film 22 and the capacitor sections to cover the interlayer plasma oxide film 22 and the capacitor sections. An opening 36 for a connection with the bit contact 30 is formed with a lithography and dry etching technique on the upper surface of the contact portion metal plug 18' to extend from the surface of the oxide film 35 to the contact portion metal plug 18' through the silicon oxynitride film 21, the interlayer plasma oxide film 22 and the oxide film 35.

[0074]

Next, as shown in Fig.12, the formed opening 36 for the connection with the bit contact 30 is plugged with tungsten so as to form the bit contact 30. An end of this bit contact 30 is connected with the upper portion of the contact portion metal plug 18'. Another end of the contact

portion metal plug 18' is connected with the bit line 31, which extends along the surface of the oxide film 35. The thus-described manufacturing process completes a DRAM.

[0075]

In this way, the semiconductor memory device according to the embodiment 1 reduces the contact resistance and the contact plug resistance through forming capacitor contact portions (the capacitor contact holes 17) and a bit contact portion (the cell contact hole 18) at the same time, and forming the contact plugs in connection with the capacitor contact portions and the bit contact portion with metal plugs (the contact portion metal plugs 17', the contact portion metal plug 18'). Additionally, the semiconductor memory according to the embodiment 1 provides barrier metal to avoid the contact portion metal plug 17' and the DOPOS layer 25 being directly reacted through forming the bottom electrode 6 with the dual layered stack of the titanium nitride layer 23 and the DOPOS layer 25, and also provides low resistance electrodes. Furthermore, the semiconductor memory according to the embodiment 1 reduces the aspect ratio in connection with the bit contact etching by forming the cell contact 18 under the bit contact 30.

[0076]

As described above, the semiconductor memory device according to the embodiment 1, which reduces the contact resistance and the contact plug resistance through forming capacitor contact portions (the capacitor contact holes 17) and a bit contact portion (the cell contact hole 18) at the

same time, and forming the contact plugs in connection with the capacitor contact portions and the bit contact portion with metal plugs (the contact portion metal plugs 17', the contact portion metal plug 18'), provides contribution for reducing the electric power consumption, and achieves the high-speed operation. Also, the semiconductor memory device according to the embodiment 1, which provides barrier metal to avoid the contact portion metal plug 17' and the DOPOS layer 25 being directly reacted through forming the bottom electrode 6 with the dual layered stack of the titanium nitride layer 23 and the DOPOS layer 25, and also provides low resistance electrodes, provides contribution for reducing the electric power consumption, and achieves the high-speed operation.

[0077]

Furthermore, in the semiconductor memory device according to the embodiment 1, which reduces the aspect ratio in connection with the bit contact etching by forming the capacitor contact portion (capacitor contact holes 17) and the bit contact portion (the cell contact 18) at the same time, achieves improved productivity in addition to the aforementioned reduced electric consumption and the high-speed operation.

[0078]

Also, the semiconductor memory device according to the embodiment 1 facilitates the etching process through reducing the aspect ratio of the bit contact by forming the cell contact below the bit contact.

[0079]

(Second Embodiment)

In the manufacturing process of the semiconductor memory device (DRAM) according to the embodiment 1, the capacitor contact portions (the capacitor contact holes 17) and the bit contact portion (the cell contact hole 18) are formed at the same time so as to improve productivity. Additionally, in the embodiment 2, contact portions of a semiconductor memory device (the DRAM section) and the peripheral logic section are opened at the same time and contact plugs are embedded at the same time, so that the productivity is further improved in addition to the effect in the embodiment 1.

[0080]

The semiconductor memory device according to the embodiment 2 is described below with reference to Fig. 13. It should be note that the structure of the semiconductor memory device according to the embodiment 2 is identical to that in the embodiment 1 and the description thereof is therefore omitted. Also, the structures corresponding to the semiconductor memory device in the peripheral logic section are denoted by the same numerals.

[0081]

Fig. 13 is a cross-section view illustrating a structure of a semiconductor memory device according to the embodiment 2 and the structure of the peripheral logic section.

[0082]

As shown in Fig. 13, a diffusion layer region is formed in the surface portion of the P-type silicon substrate 50 within the peripheral logic section. STI oxide films 1, LDDs (lightly doped drain) 11 and 11', N-type source diffusion layers 13 are formed in the surface portion of this P-type silicon substrate 50 in pairs. The STI oxide films 1 are disposed to electrically insulate the adjacent diffusion layer regions. It should be noted that LDDs 11 and 11' are formed in a single process. The STI oxide films 1 and the source diffusion layers 13 are connected each other. The LDDs 11 and the source diffusion layers 13 are connected each other. Insulating films 32 are formed on the surfaces of the source diffusion layers 13. Additionally, an N-type drain diffusion layer 14 is formed in the surface portion of the P-type silicon substrate 50. The one of the aforementioned LDDs 11' and the drain diffusion layer 14 are connected each other. Also, the other LDD 11' and the drain diffusion layer 14 are connected each other. An insulating film 32' is formed on the surface of the drain diffusion layer 14. It should be noted that insulating films 32 and 32' are formed in a single process. Direct nitride films 15 are formed on the surfaces of the STI oxide films 1 and the insulating films 32.

[0083]

Gate oxide films 9 are formed on the P-type silicon substrate 50. Gates 10 are formed on the surfaces of the gate oxide films 9. Insulating films 33 are formed on the surface portion of the gates 10. Sidewalls 12 are formed on

the surfaces of LDDs 11 and 11'. The sidewalls 12 are connected with the LDDs 11 and 11', the gates 10, the insulating films 33. Direct nitride films 15' are formed on the sidewalls 12, the insulating films 33, the insulating film 32'. It should be noted that the direct nitride films 15 and 15' are formed in a single process. Thus, MOS transistors are formed in the surface portion of the P-type silicon substrate 50. A buried oxide film 16 is formed on the surfaces of the direct nitride films 15 and 15' to cover the aforementioned MOS transistors.

[0084]

Contact portion metal plugs 17' are formed on the source diffusion layers 13 to extend to the surface of the buried oxide film layer 16 in the perpendicular direction. A contact portion metal plug 18' is formed on the drain diffusion layer 14 to extend to the surface of the buried oxide film 16 in the perpendicular direction. The contact portion metal plugs 17' and the contact portion metal plugs 18' are composed of a titanium nitride layer 19 as a barrier metal layer, a refractory metal tungsten layer 20. A oxide film 62 is formed on the surface of the buried oxide film 16, contact portion metal plug 17', the contact portion metal plug 18' to cover the buried oxide film 16, the contact portion metal plug 17', the contact portion metal plug 18'

[0085]

Bit contacts 63 are formed on the top of the contact portion metal plugs 17' to reach the surface of oxide film 62 in the perpendicular direction through the oxide film 62.

The bit contacts 63 are plugged with tungsten. Additionally, bit lines 64 are connected with the upper portion of the bit contacts 63 to extend along the surface of the oxide film 62. The bit line 64 is formed with titanium nitride. The bit contacts 63 functions as bit lines for provide connections to the bit line 64.

[0086]

Also, a bit contact 60 is formed on the top of the contact portion metal plug 18' to extend to the surface of oxide film 62 through the oxide film 62. The bit contact 60 is plugged with tungsten. Additionally, a bit line 61 is connected to the upper portion of the bit contact 60 to extend along the surface of the oxide film 62. The bit contact 60 functions as a bit line for provide connections to the bit line 61.

[0087]

In this way, the semiconductor memory device and the peripheral logic section are designed to allow the contact plugs (the contact portion metal plugs 17', and the contact portion metal plug 18') to be formed at the same time, and to allow the bit contacts (the bit contact 30, the bit contacts 60, the bit contact 63) to be formed at the same time.

[0088]

Next, a manufacturing process of the semiconductor memory device and the peripheral logic section according to the above mentioned embodiment 2 is described bellow with reference to the Fig. 14, Fig. 15. It should be noted that

the manufacturing process of the semiconductor memory device according to the embodiment 2 is identical to that in the embodiment 1.

[0089]

Fig. 14 is a cross-section view illustrating the manufacturing process of the semiconductor memory device and the peripheral logic section according to the embodiment 2.

[0090]

Fig. 15 is a cross-section view illustrating the manufacturing process of the semiconductor memory device and the peripheral logic section according to the embodiment 2.

[0091]

As shown in Fig. 14, STI oxide films 1 of 3500 Å in depth for isolation are formed on a P-type silicon substrate 50 for the semiconductor memory device and the peripheral logic section. A well is formed in the surface portion of the P-type silicon substrate 50 by an ion implantation. After forming gate oxide films 9 of 70 Å in thickness, DOPOS of 1500 Å in thickness is deposited, and gates 10 are formed through a lithography and plasma etching technique. LDDs 11 are formed through implantation in the surface portion of the P-type silicon substrate 50. After the implantation for forming the LDDs 11, sidewalls 12 are formed on the surfaces of the LDDs 11. Additionally, source diffusion layers 13 and a drain diffusion layer 14 are formed in the surface portion of the P-type silicon substrate 50 by an ion implantation. The gates 10, the source diffusion layers 13, and the drain diffusion layer 14 are then subjected to a

cobalt silicide process. Also, insulating films 33 are formed on the surfaces of the gates 10, insulating films 32 are formed on the surfaces of the source diffusion layers 13, and an insulating film 32' is formed on the surface of the drain diffusion layer 14.

[0092]

Next, the surfaces of the STI oxide films 1 and the insulating films 32 are covered with direct nitride films 15. The surfaces of the insulating films 32, the sidewalls 12 and the insulating films 33, and the insulating film 32' are covered with direct nitride films 15' of 400 Å in thickness. Moreover, the surfaces of the direct nitride films 15 and 15' are covered with an oxide film 16 of 6000 Å in thickness. Contact holes are opened on the surfaces of both of the source diffusion layers 13 and the drain diffusion layer 14 at the same time by lithography and dry etching techniques. That is, capacitor contacts are opened to expose the surfaces of the source diffusion layers 13, and to extend upward in the perpendicular direction, and a cell contact is opened to expose the surface of the drain diffusion layer 14 and to extend upward in the perpendicular direction at the same time.

[0093]

Then, side and bottom portions of the capacitor contacts and the cell contact are covered with a titanium nitride layer 19 to be a barrier metal layer, and a tungsten layer 20 of the refractory metal is embedded inside the titanium nitride layers 19, which is formed inside both of

the capacitor contacts and the cell contact. Also, after the deposition of the titanium nitride layer 19 and the tungsten layer 20, the contact portion metal plugs 17' are formed with the titanium nitride layer 19 and the tungsten layer 20 inside the capacitor contacts through a tungsten etchback or CMP process, while the contact portion metal plug 18' is formed with the titanium nitride layer 19 and the tungsten layer 20 inside the cell contact.

[0094]

Next, as shown in Fig.15, a silicon oxynitride film 21 of 500 Å in thickness is deposited on the surface of the buried oxide film 16, contact portion metal plugs 17' and the contact portion metal plug 18' for the semiconductor memory device. After the deposition of the silicon oxynitride film 21, a cylinder interlayer film is formed with a plasma oxide film 22 of 10000 Å in thickness on the surface of the silicon oxynitride film 21. Openings are formed with lithography and dry etching techniques through etching downward to reach from the surface of the cylinder interlayer film (the plasma oxide film 22) to the surface of the silicon oxynitride film 21 for etching stopper in the perpendicular direction with respect to the contact portion metal plugs 17'. In order to remove the silicon oxynitride film 21 for the stopper, the silicon oxynitride film 21 is etched to allow the openings to reach the contact portion metal plugs 17'.

[0095]

A titanium nitride layer 23 of 100 Å in thickness for

the bottom electrodes 6 is deposited on the openings, which are positioned over the contact portion metal plugs 17', and resist material is left only inside the cylinders. The titanium nitride layer 23 is formed only inside the cylinders for the openings 34 through an etchback process with dry etching.

[0096]

After removing the resist material, a DOPOS layer 25 is then deposited on the side surface of the openings, which are covered with the titanium nitride layer 23. The surfaces of the openings, on which the DOPOS layer 25 is deposited, are subjected to a HSG process. Then, resist material is left only inside the cylinders on the HSG-processed surfaces of the openings. The HSG-processed DOPOS layer 25 is formed only inside the cylinders through an etchback with dry etching. The titanium nitride layer 23 should be formed to have a reduced height through the preceding processes so as not to be exposed. After that, the bottom electrodes 6 are completed by removing the resist material 26 in the cylinders of the openings, on which the DOPOS layer 25 is formed.

[0097]

Next, Ta_2O_5 capacitor films 27 of high dielectric constant material as dielectric layers are deposited on the surfaces of the bottom electrodes 6 to have a thickness of 80 Å. Titanium nitride layers 28 of 100 Å in thickness and the DOPOS 29 of 1500 Å in thickness are deposited on the surfaces of the Ta_2O_5 capacitor films 27 as the upper

electrodes 8. This completes the above mentioned capacitor sections. An oxide film 35 is formed on the surface of the interlayer plasma oxide film 22 and the capacitor sections to cover the interlayer plasma oxide film 22 and the capacitor sections.

[0098]

On the other hand, for the peripheral logic section, an oxide film 62 is formed on the surface of the buried oxide film 16, the contact portion metal plugs 17' and the contact portion metal plug 18' to cover the buried oxide film 16, the contact portion metal plugs 17' and the contact portion metal plug 18'.

[0099]

Openings for the bit contact connections are formed at the same time by lithography and the dry etching techniques for the semiconductor memory device and the peripheral logic section. In other words, for the semiconductor memory device, an opening for a connection with the bit contact 30 is formed on the contact metal plug 18' to extend from the surface of the oxide film 35 to the contact portion metal plug 18' through the silicon oxynitride film 21, the interlayer plasma oxide film 22 and the oxide film 35. At the same time, for the peripheral logic, an opening for a connection with the bit contact 60 is formed on the contact portion metal plugs 17' to extend from the surface of the oxide film 62 to the contact portion metal plug 17' through the oxide film 62. Moreover, at the same time, for the peripheral logic section, openings for

connections with the bit contacts 63 are formed on the contact portion metal plug 18' to extend from the surface of the oxide film 62 to the contact portion metal plug 18'.

[0100]

Next, for the semiconductor memory device, the opening for the connection with the formed bit contact 30 is plugged with tungsten so as to complete the bit contact 30. An end of the bit contact 30 is connected with the upper portion of the contact portion metal plug 18' in the semiconductor memory device. At the same time, for the peripheral logic section, the openings for connections with the formed bit contacts 60 and 63 are plugged with tungsten so as to complete the bit contacts 60 and 63. An end of the bit contact 60 is connected with the upper portion of the contact portion metal plug 18' in the peripheral logic section. Ends of the bit contacts 63 are connected with the upper portions of the contact portion metal plugs 17' in the peripheral logic section. The bit line 31 is connected with the other end of the bit contact 30 to extend along the surface of the oxide film 35 in the semiconductor memory device. Also at the same time, the bit line 61 is connected with the other end of the bit contact 60 to extend along the surface side of the oxide film 62, and the bit lines 64 are connected with the other ends of the bit contacts 63 to extend along the surface of the oxide film 62 in the peripheral logic section.

[0101]

As thus described, the semiconductor memory device according to the embodiment 2 achieves further improvement of productivity in additional to the effect by the embodiment 1 through forming the contact portions of the semiconductor memory device and the peripheral logic sections at the same time and plugging the contact plugs at the same time.

[0102]

[Effect of the invention]

The semiconductor memory according to the present invention contributes reduction in the electric power consumption, and achieves high-speed operation.

[Brief Description of the drawings]

[Fig.1]

Fig.1 is a cross-section view illustrating the structure of the semiconductor memory device according to the embodiment 1.

[Fig.2]

Fig. 2 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.3]

Fig. 3 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.4]

Fig. 4 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.5]

Fig. 5 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.6]

Fig. 6 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.7]

Fig. 7 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.8]

Fig. 8 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.9]

Fig. 9 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the

embodiment 1.

[Fig.10]

Fig. 10 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.11]

Fig. 11 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.12]

Fig. 12 is a cross-section view illustrating the manufacturing process in connection with the manufacturing method of the semiconductor memory device according to the embodiment 1.

[Fig.13]

Fig. 13 is a cross-section view illustrating the manufacturing process of the semiconductor memory device and the peripheral logic section according to the embodiment 2.

[Fig.14]

Fig. 14 is a cross-section view illustrating the manufacturing process of the semiconductor memory device and the peripheral logic section according to the embodiment 2.

[Fig.15]

Fig. 15 is a cross-section view illustrating the manufacturing process of the semiconductor memory device and the peripheral logic section according to the embodiment 2.

[Fig.16]

Fig. 16 is a cross-section view illustrating the structure of the conventional semiconductor memory device.

[Description of the reference Numerals and Symbols]

1 STI oxide film

6 bottom electrode

8 upper electrode

9 gate oxide film

10 10 gate

11 LDD

11' LDD

12 sidewall

13 source diffusion layer

15 14 drain diffusion layer

15 direct nitride film

15' direct nitride film

16 buried oxide film

17 capacitor contact

20 17' contact portion metal plug

18 cell contact

18' contact portion metal plug

19 titanium nitride layer (The barrier metal layer)

20 tungsten layer

25 21 silicon oxynitride film for stopper

22 interlayer plasma oxide film

23 tail electrode (titanium nitride layer)

24 resist material for the titanium nitride protection

etching back

25 tail electrode (DOPOS layer)

26 resist material for the polysilicon protection etching back

27 Ta_2O_5 capacitor film

28 upper electrode (titanium nitride layer)

29 upper electrode (DOPOS layer)

30 bit contact (tungsten plug)

31 bit line (titanium nitride)

32 insulating film

32' insulating film

33 insulating film

34 opening

35 oxide film

36 opening

50 silicon substrate (P type)

60 bit contact

61 bit line (titanium nitride)

62 oxide film

63 bit contact

64 bit line (titanium nitride)

100 silicon substrate (P type)

101 STI oxide film

102 bit contact

103 gate

104 capacitor contact

105 polysilicon layer

106 tail electrode (polysilicon layer)

107 Ta_2O_5 capacitor film

108 upper electrode (titanium nitride layer)

109 upper electrode (polysilicon layer)

110 gate oxide film

111 LDD

111' LDD

112 sidewall

113 source diffusion layer

114 drain diffusion layer

115 direct nitride film

115' direct nitride film

116 buried oxide film

122 oxide film

131 bit line (titanium nitride)

132 insulating film

133 insulating film

133' insulating film

135 oxide film

[Document Name] Abstract

[Abstract]

[Object] To provide a semiconductor memory device and a manufacturing method of the same which contribute to reduction in electric power consumption and achieve high speed operation.

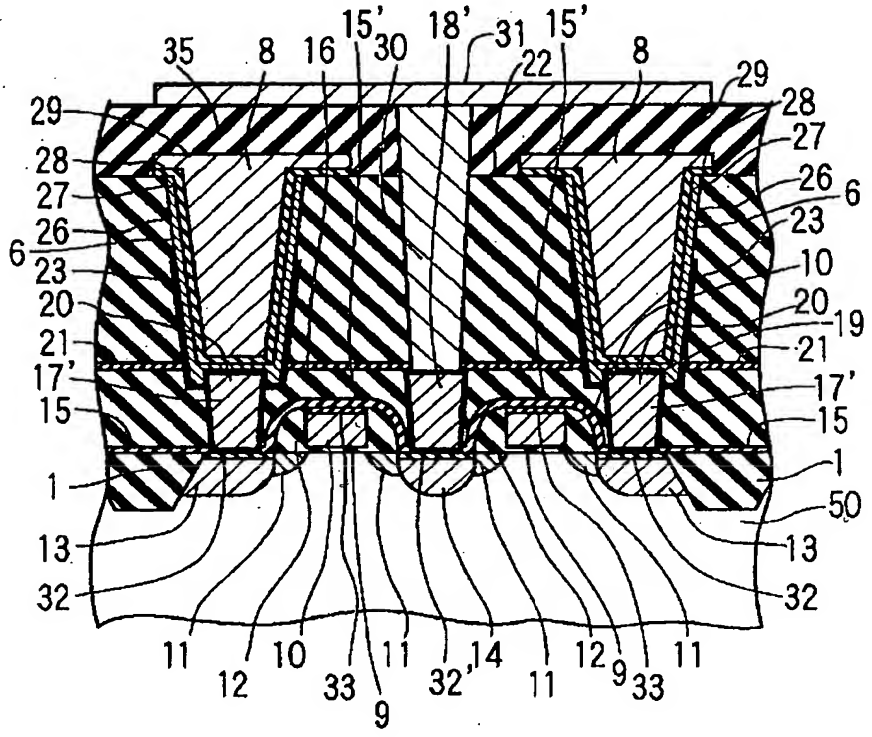
[Solving Means] The semiconductor memory device according to the present invention is composed of a MOS transistor formed on a surface of a semiconductor substrate (50) having

a gate (10), a source region (13), and a drain region (14), a first insulating film (16, 21, 22) covering the MOS transistor, a capacitor section formed on the first insulating film (16, 21, 22) including a bottom electrode (6), a dielectric layer formed on the bottom electrode(6), and an upper electrode (8) formed on the dielectric layer, and a first contact portion (17') formed through the first insulating film (16, 21, 22) extending from the bottom electrode (6) to the source region (13). The first contact portion (17') includes a first metal plug portion.

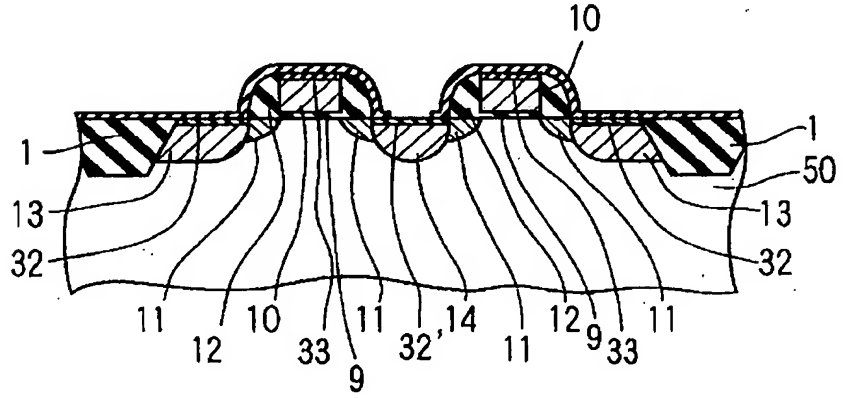
[Selected Drawing] Fig.1

【書類名】　図面　[DOCUMENT NAME] DRAWINGS

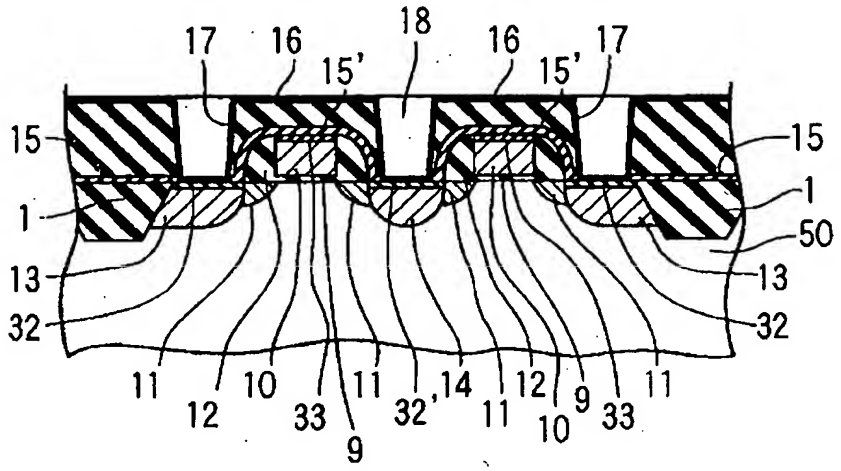
【図１】　[FIG.1]



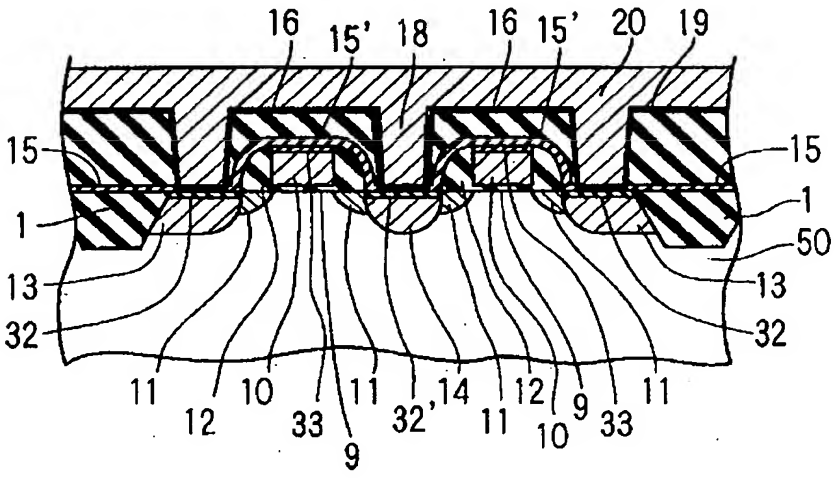
【図２】　[FIG.2]



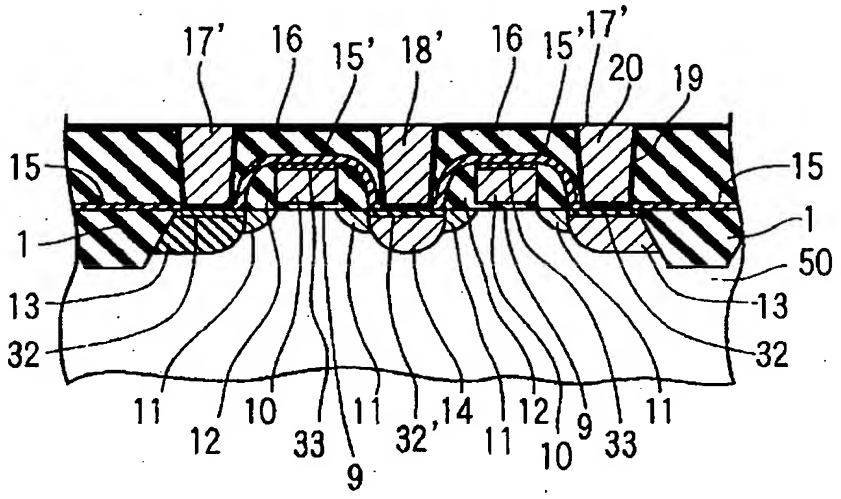
【図３】　[FIG.3]



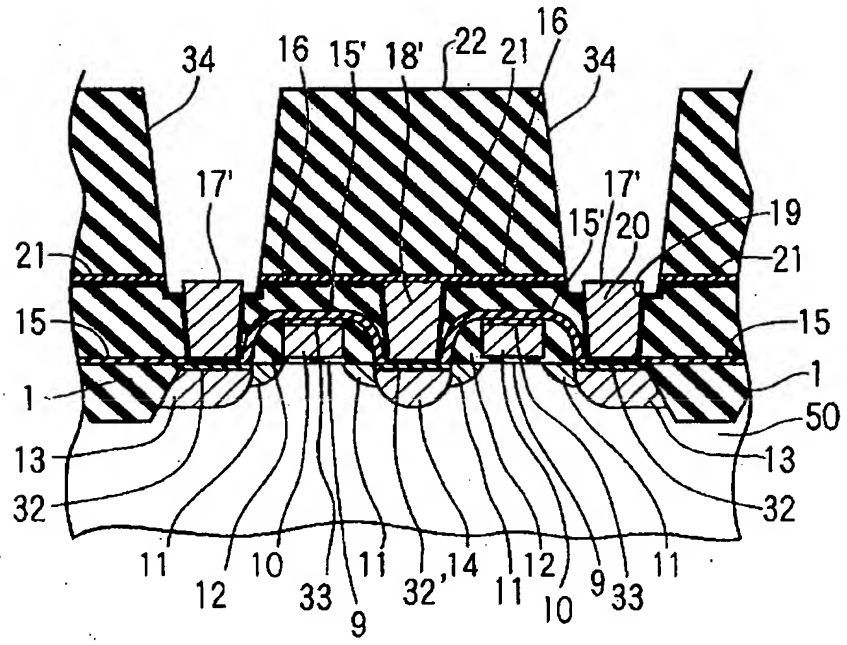
【図４】　[FIG.4]



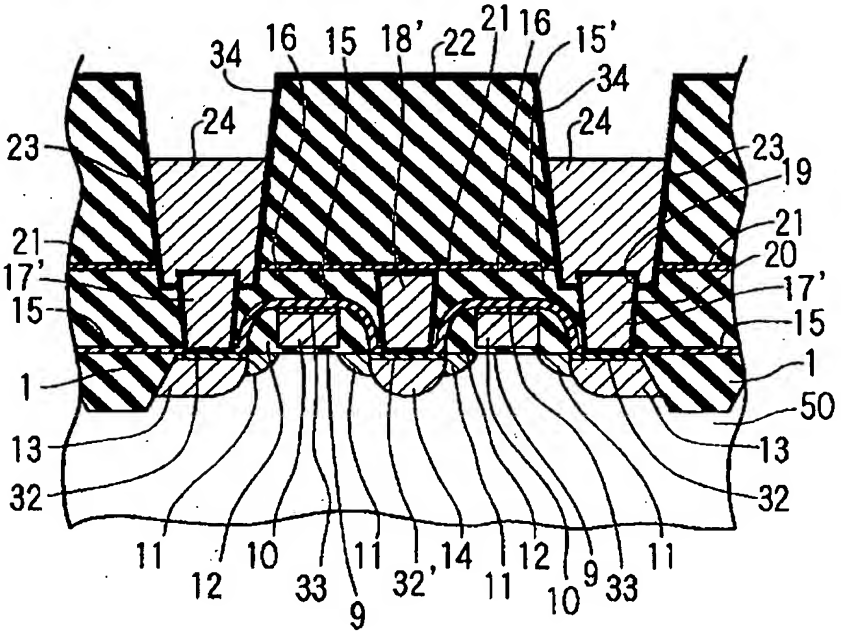
【図５】 [FIG.5]



【図６】 [FIG.6]



【図７】 [FIG.7]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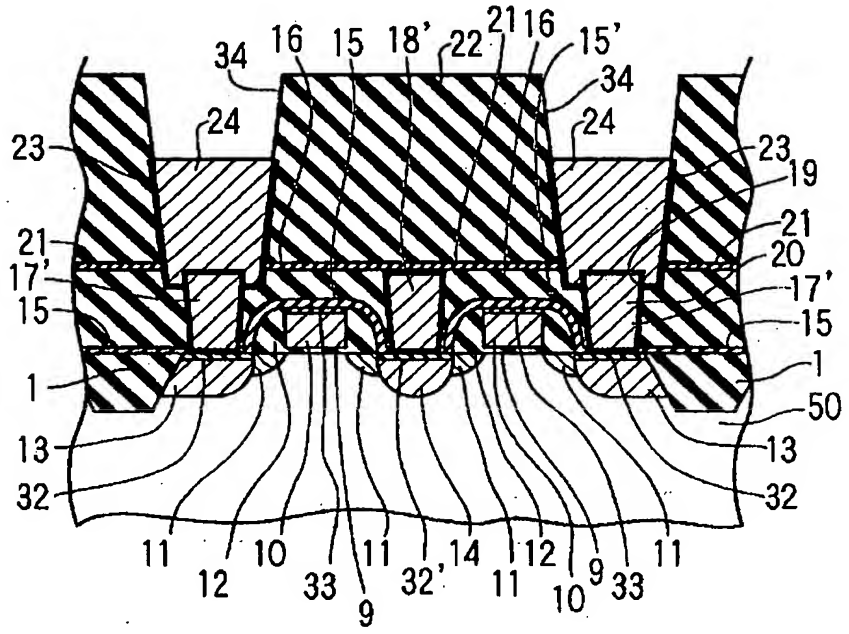
【図８】 [FIG.8]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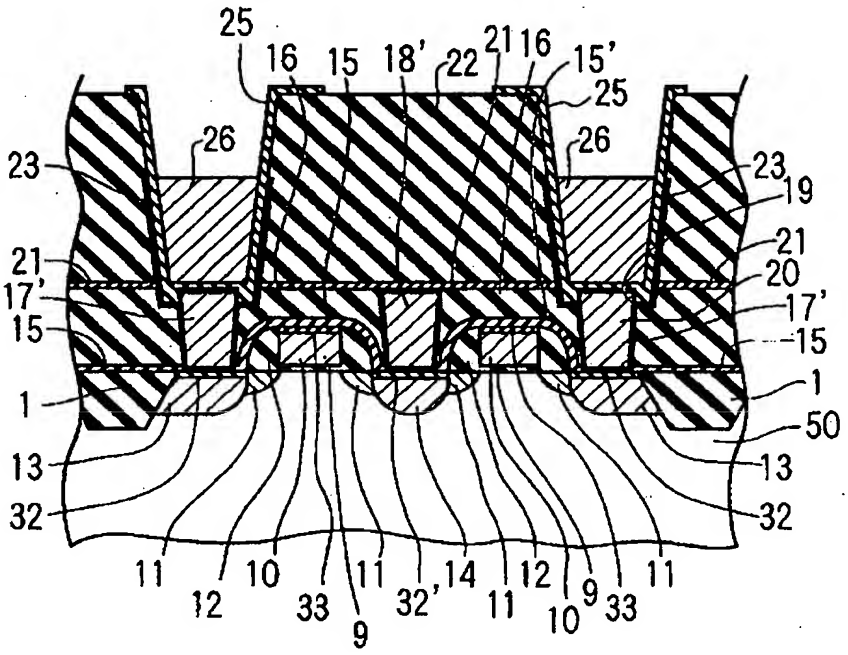
【図９】[FIG.9]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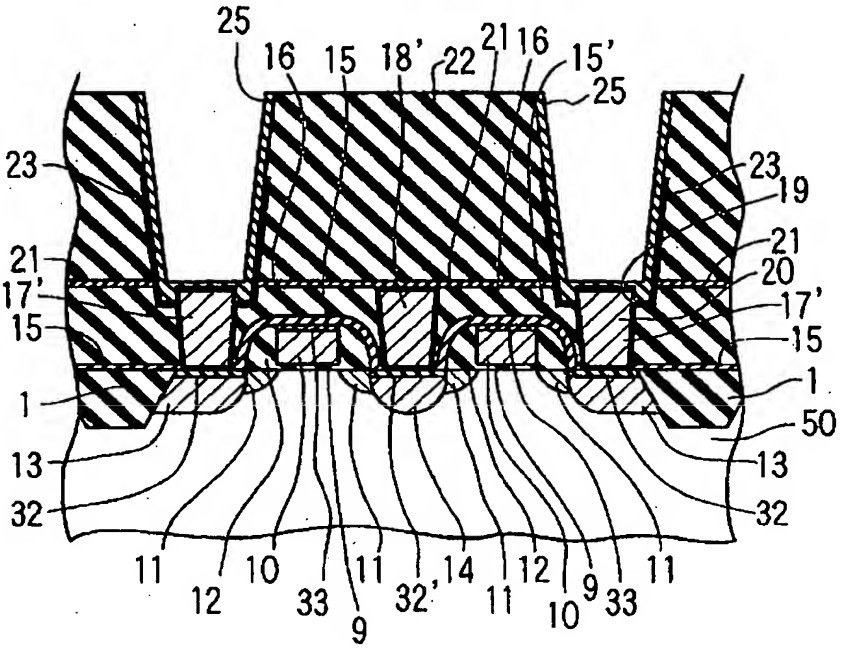
【図１０】 [FIG.10]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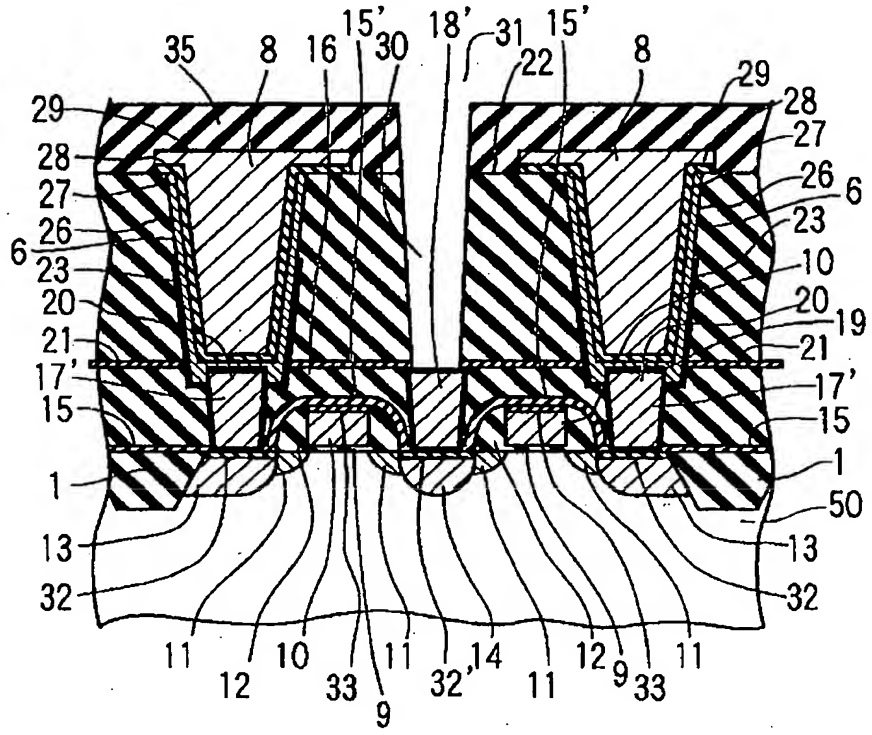
【図１１】 [FIG.11]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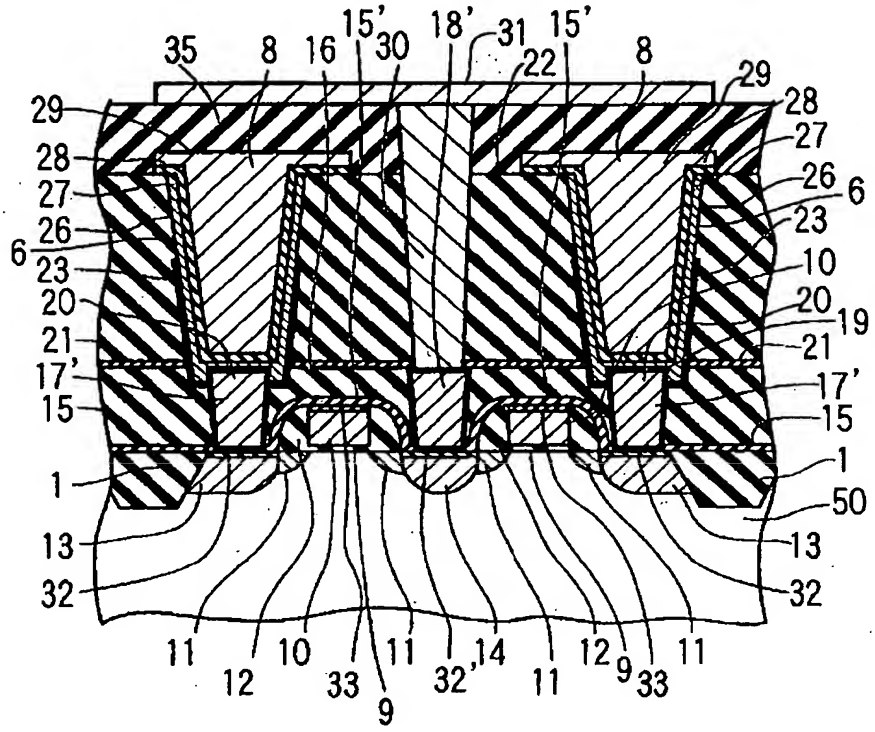
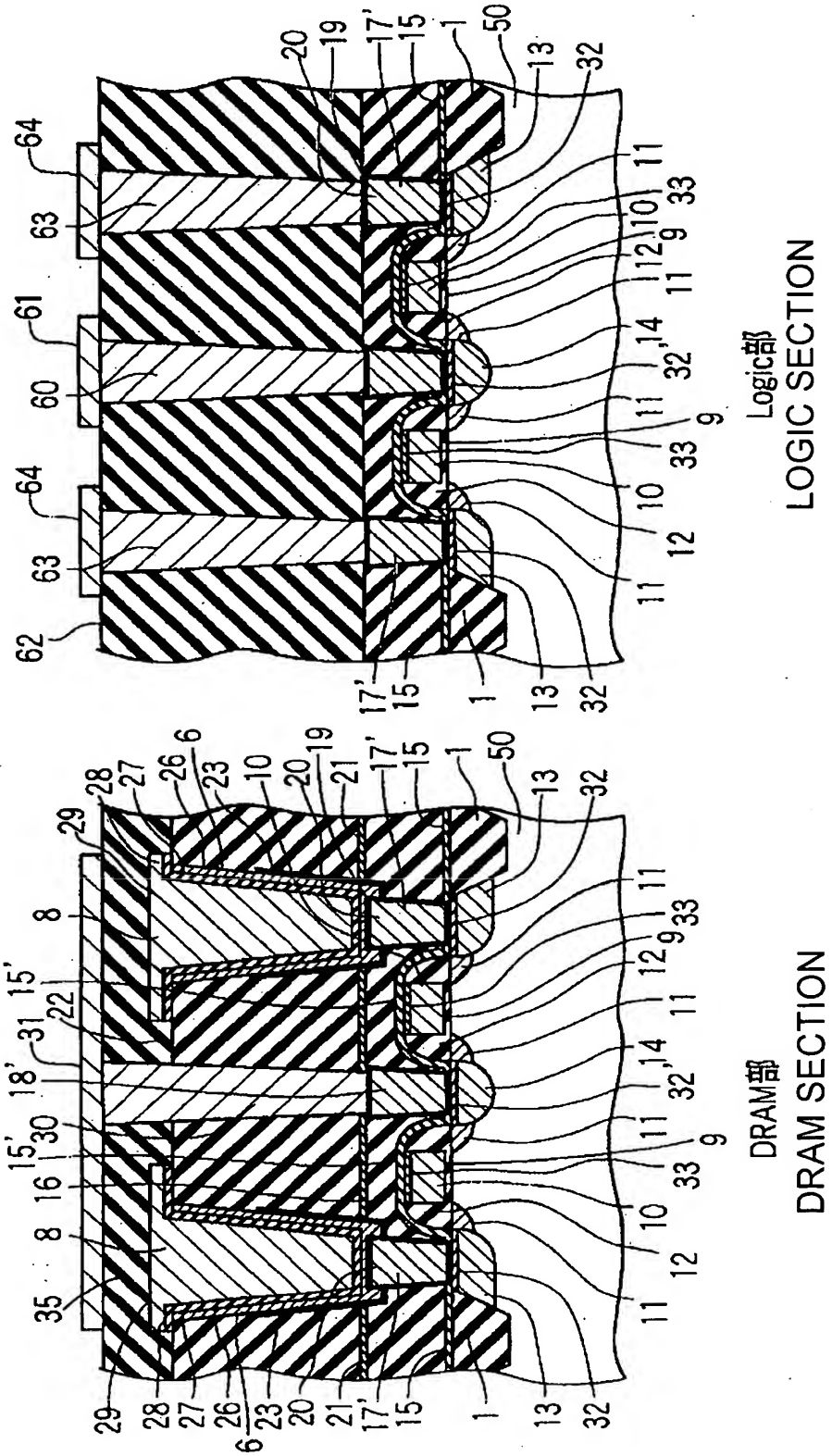
【図１２】　[FIG.12]



【図１３】　[FIG.13]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DRAM SECTION
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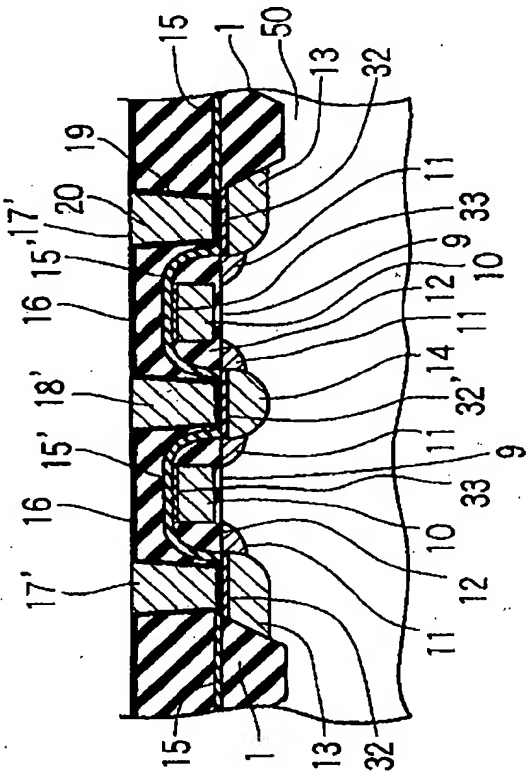
【図１４】 [FIG.14]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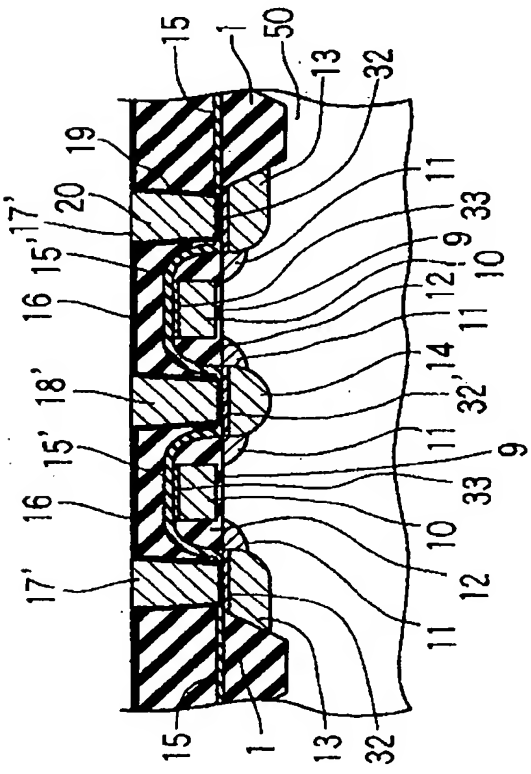
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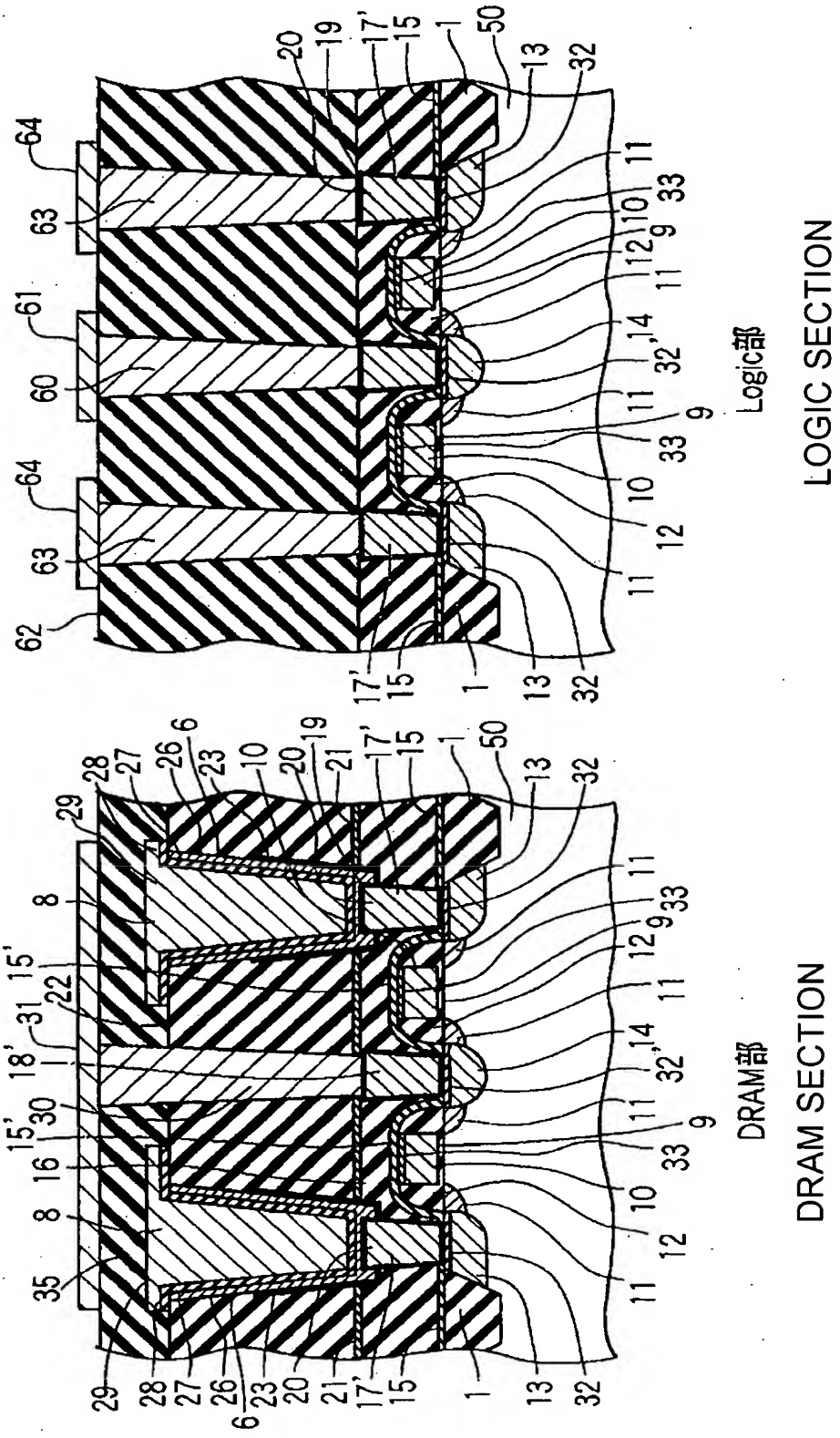
【図１５】　[FIG.15]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DRAM SECTION
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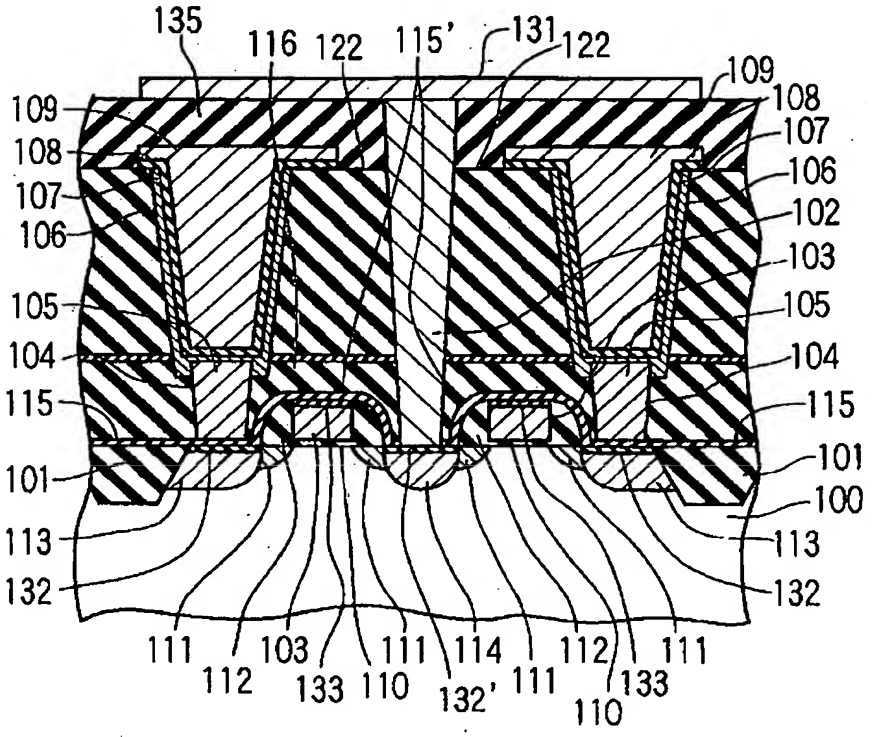
【図１６】 [FIG.16]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